sPHENIX MAPS Electronics

Mike McCumber, Pat McGaughey
Los Alamos National Laboratory

Participants and Expertise

List is still forming:

LANL P-25 (Physics), AOT (EE) Groups

UNM, BNL

Hope to draw on LBNL expertise

Expertise gained from PHENIX FVTX project and others:

Si pixel sensors and custom ASIC readout

Analog / digital electronics design and layout

High speed differential and fiber optic data transmission

Use of modern FPGAs from Xilinx, Actel

FPGA programming with Verilog and VHDL

Custom high density interconnects (FPC)

Event building and formatting

Disclaimer

We are **not** experts on the MAPS readout and have a lot of learning to do!

Becoming expert will require assistance from ALICE / LBNL members. We are becoming associate (technical) members

LANL LDRD funds will not start until October 1st. Our effort is limited until this 3-year long support arrives
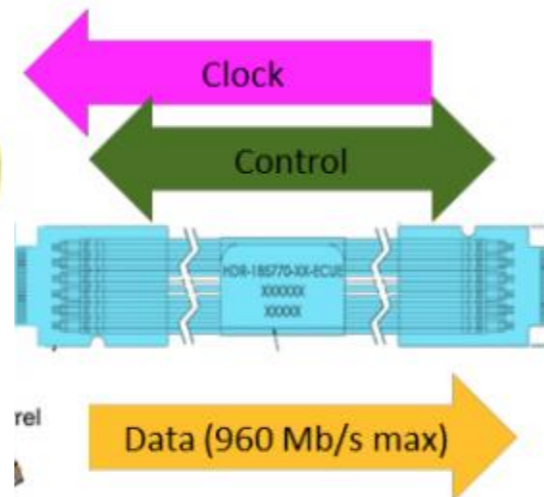
Our general approach is to reuse as much of the Alice stave and readout technology as possible. That reduces both risk and development time to meet sPHENIX schedule
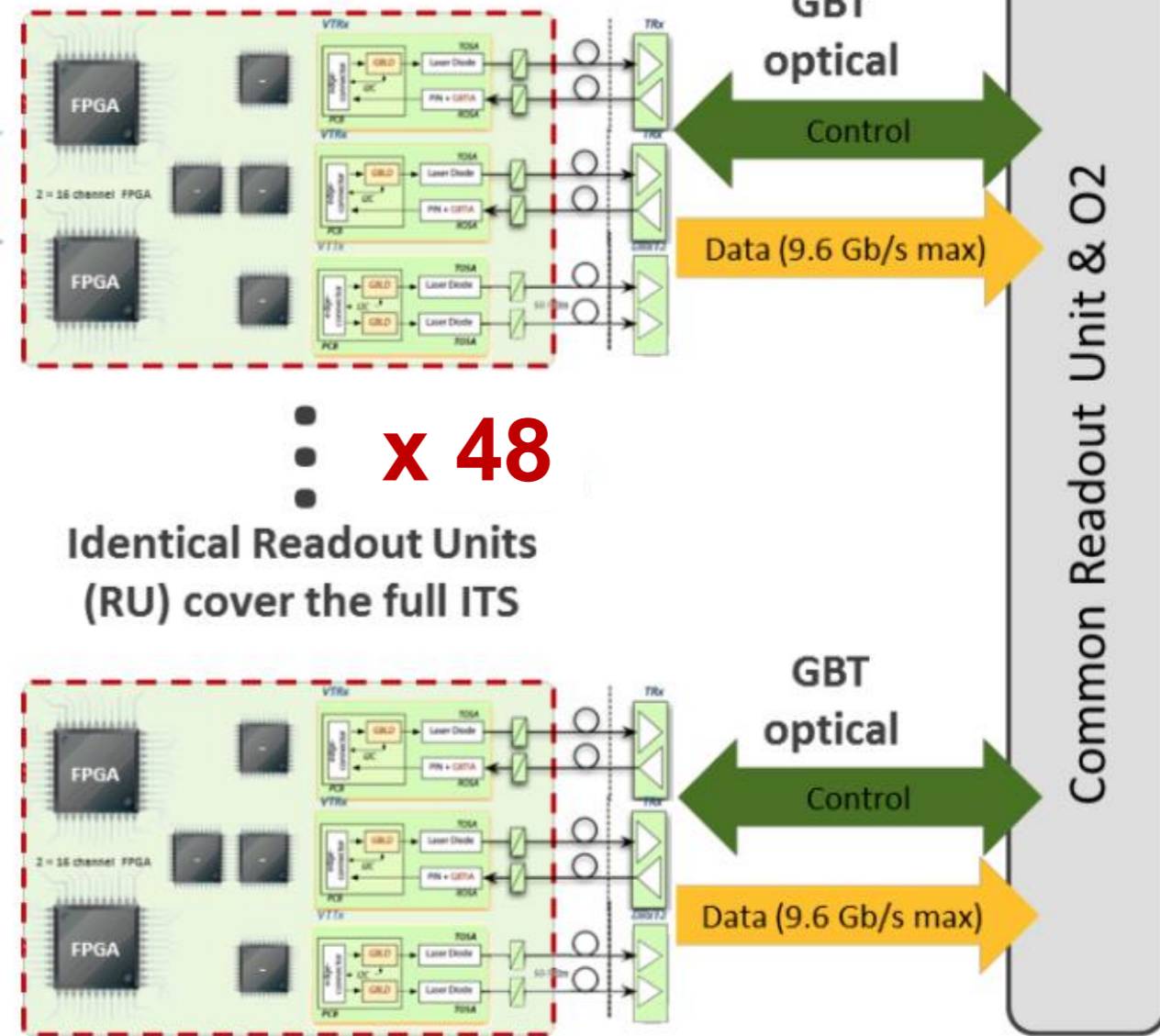
Readout Description

Staves
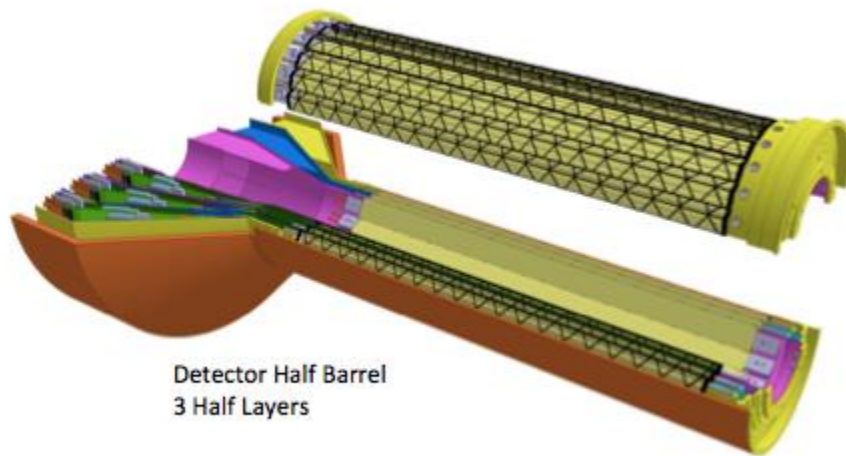
Passive electrical (copper) links, up to 1.2 Gb/s (data and control @ 40 Mb/s)
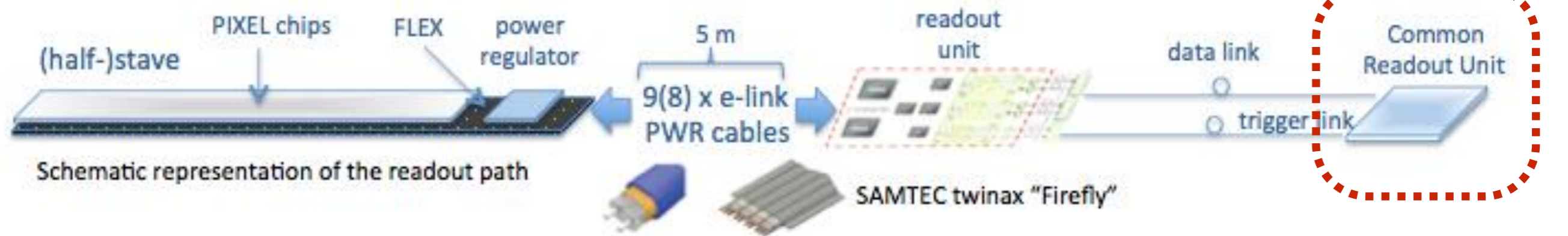
GBT optical

Trigger

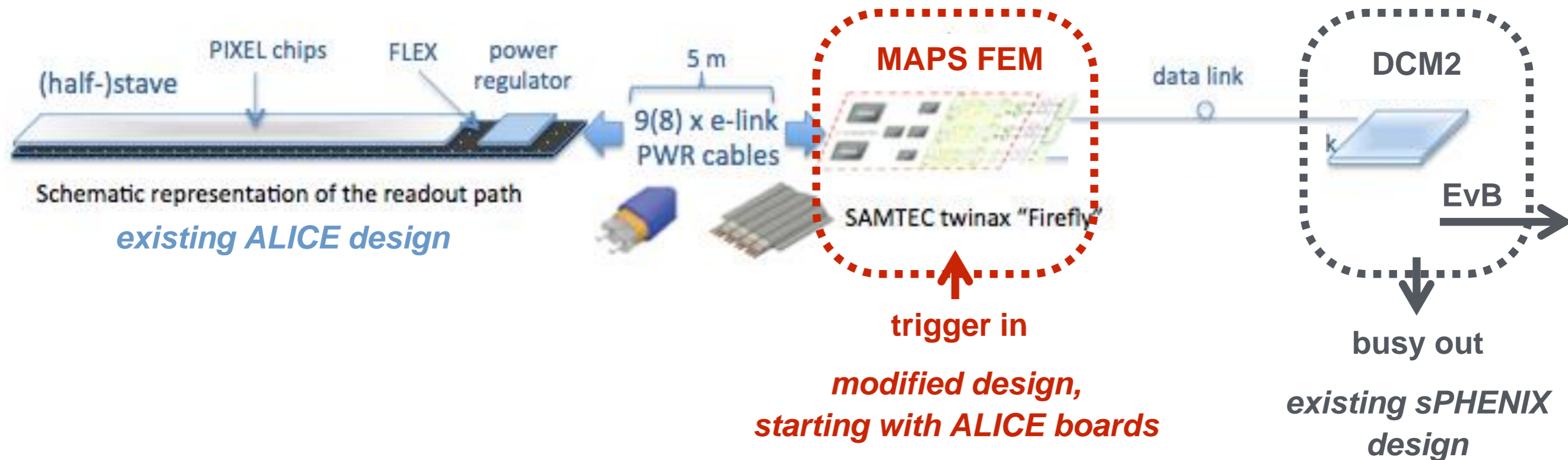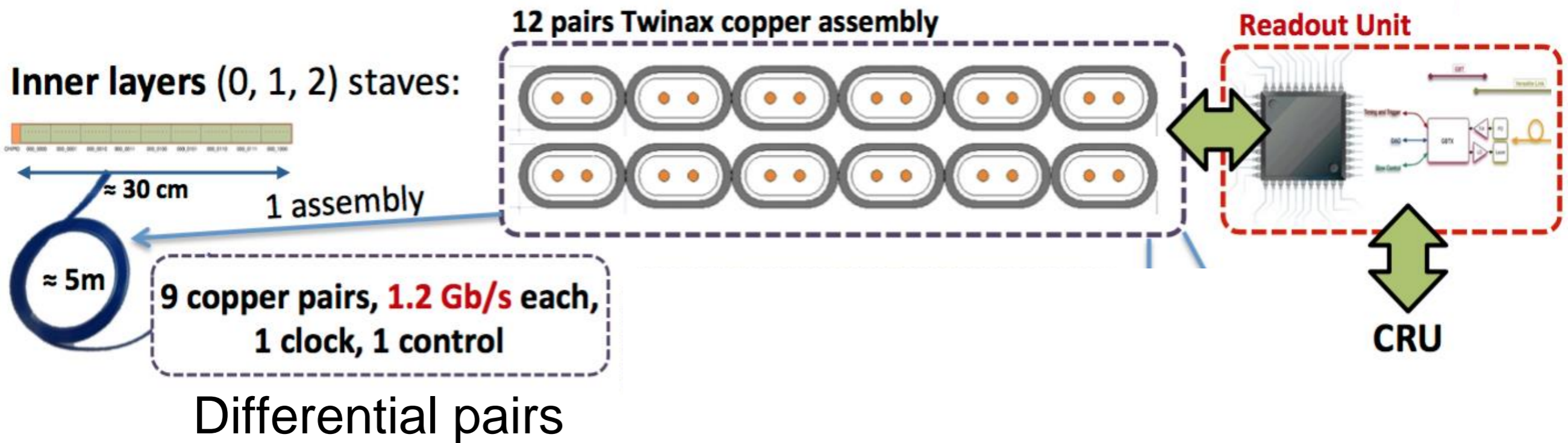One way, passive optical splitting, no busy back

x 24

Detector Half Barrel 3 Half Layers

Clock

Control

Data (960 Mb/s max)

FPGA

2 = 16 channel FPGA

FPGA

GBT optical

Control

Data (9.6 Gb/s max)

Common Readout Unit & O2

x 48

Identical Readout Units (RU) cover the full ITS

Each Readout Unit is connected to one stave, both for in Inner and Outer Barrels

Clock

Control

Data (960 Mb/s max)

FPGA

2 = 16 channel FPGA

FPGA

GBT optical

Control

Data (9.6 Gb/s max)

MAPS Electronics

ALICE readout path

Plan A: reprogram

Plan B: sPHENIX readout path (held only as contingency)

existing ALICE design

MAPS FEM

trigger in

*modified design,
starting with ALICE boards*

existing sPHENIX design

Inner Barrel Stave Readout

Alpide X9

Control (including trigger)

Clock

CHIPID   000_0000   000_0001   000_0010   000_0011   000_0100   000_0101   000_0110   000_0111   000_1000

Inner layers (0, 1, 2) staves:

≈ 30 cm

1 assembly

≈ 5m

9 copper pairs, 1.2 Gb/s each, 1 clock, 1 control

Differential pairs

12 pairs Twinax copper assembly

Readout Unit

CRU
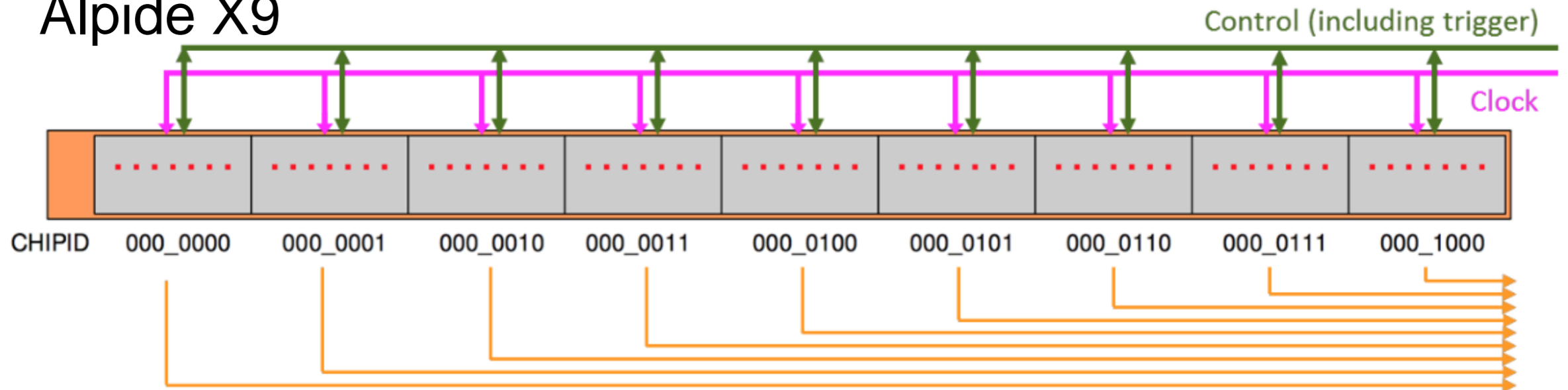
ALICE Readout Unit Logic

Schematic representation of the readout path
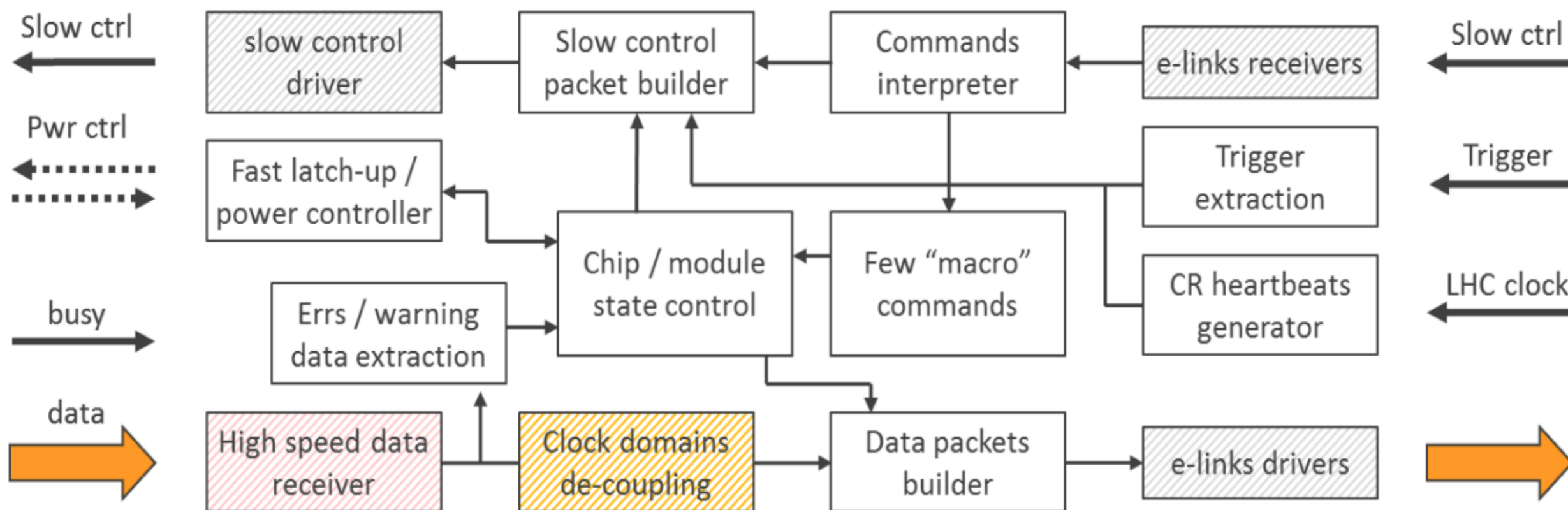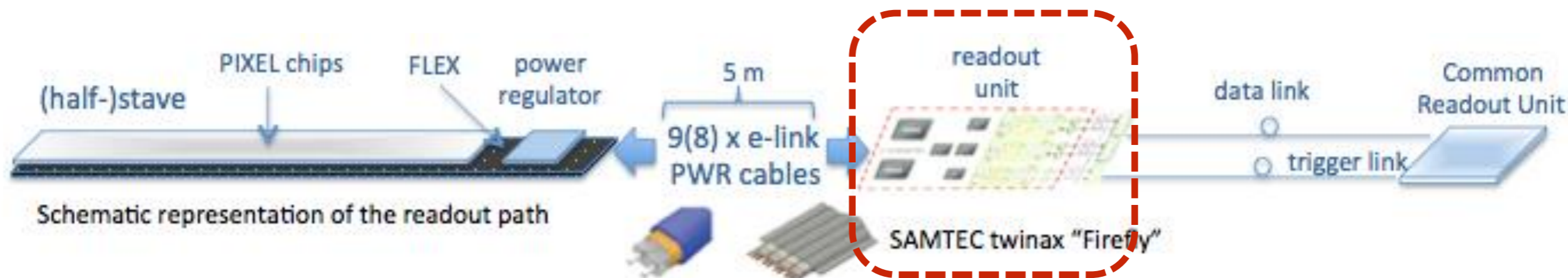
Figure 9 – Readout Electronics main functions.

ALICE Readout Units
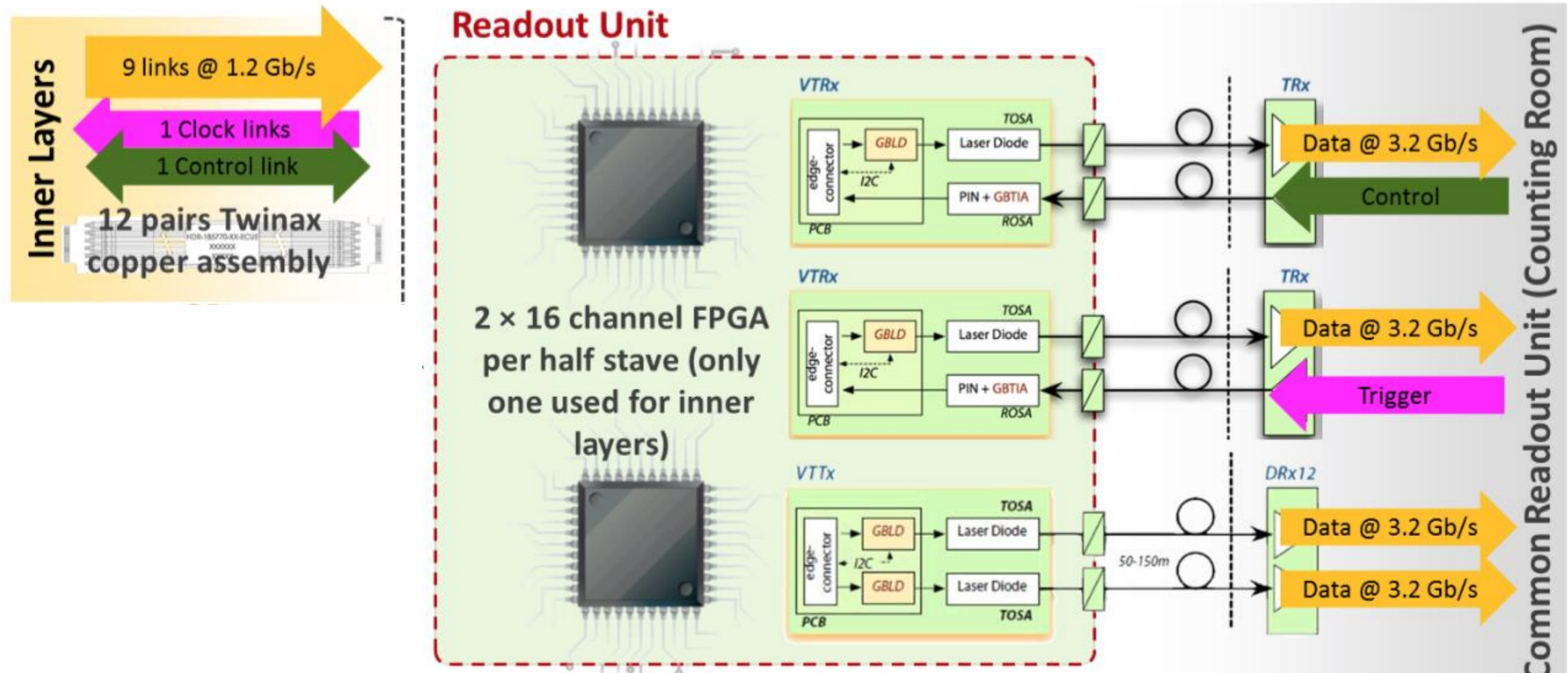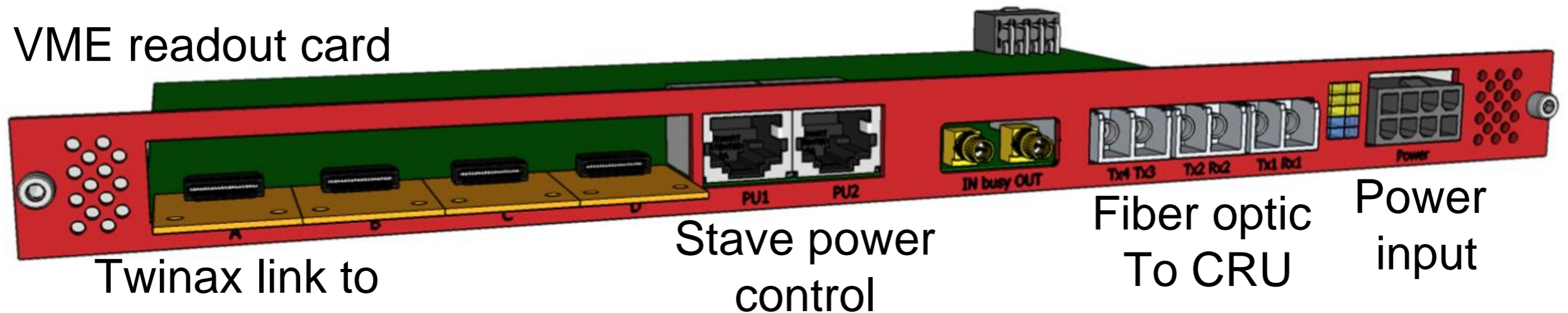
CERN Versatile Link – Bi-directional Fiberoptic

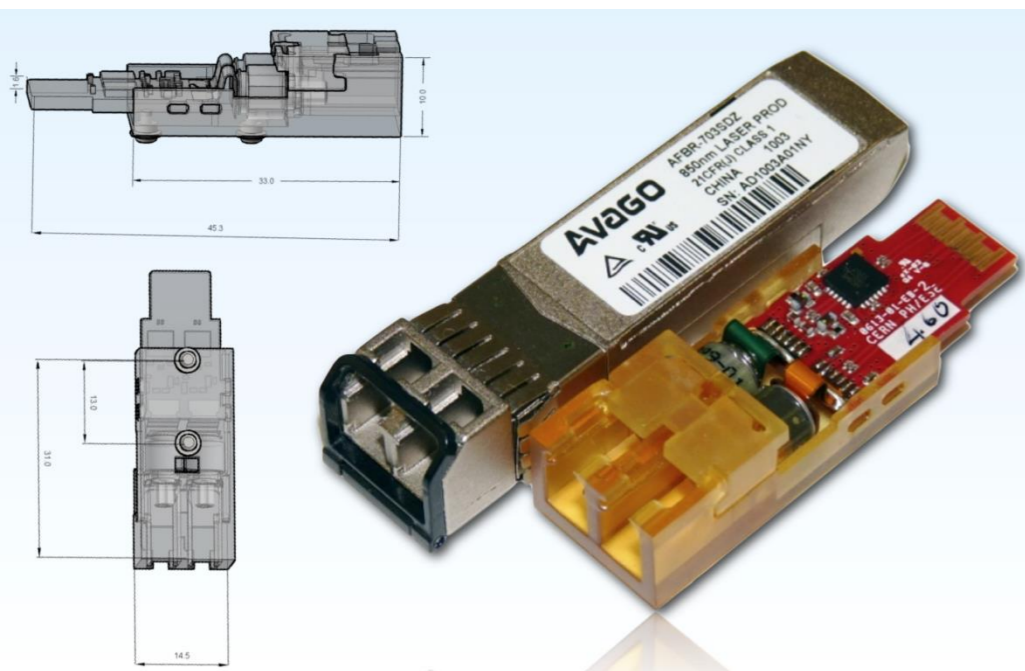3 Gb/sec up to 150 meters
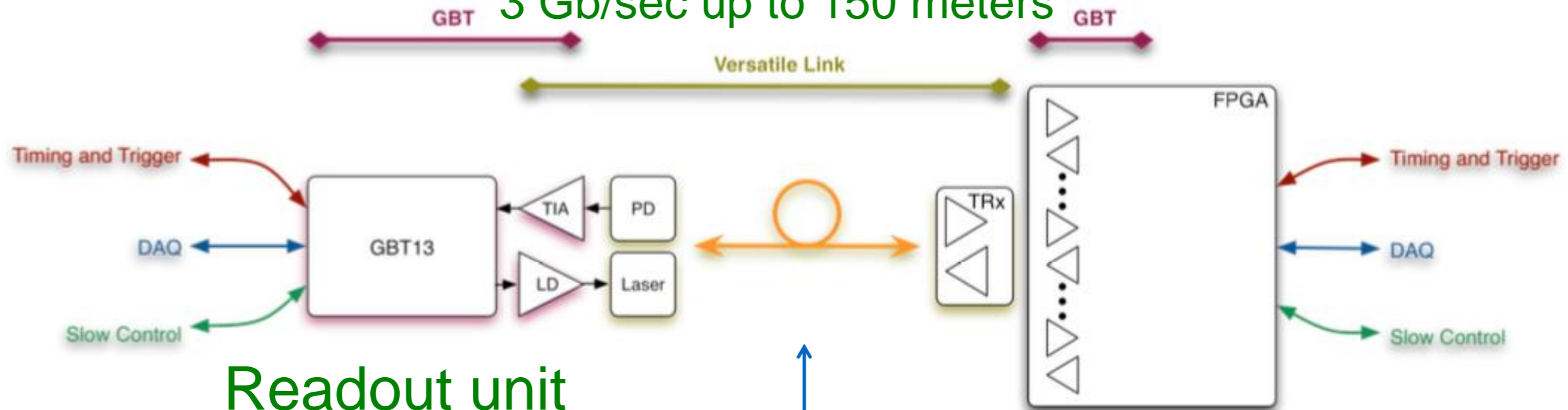
Readout unit

On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

Common readout unit
In counting house

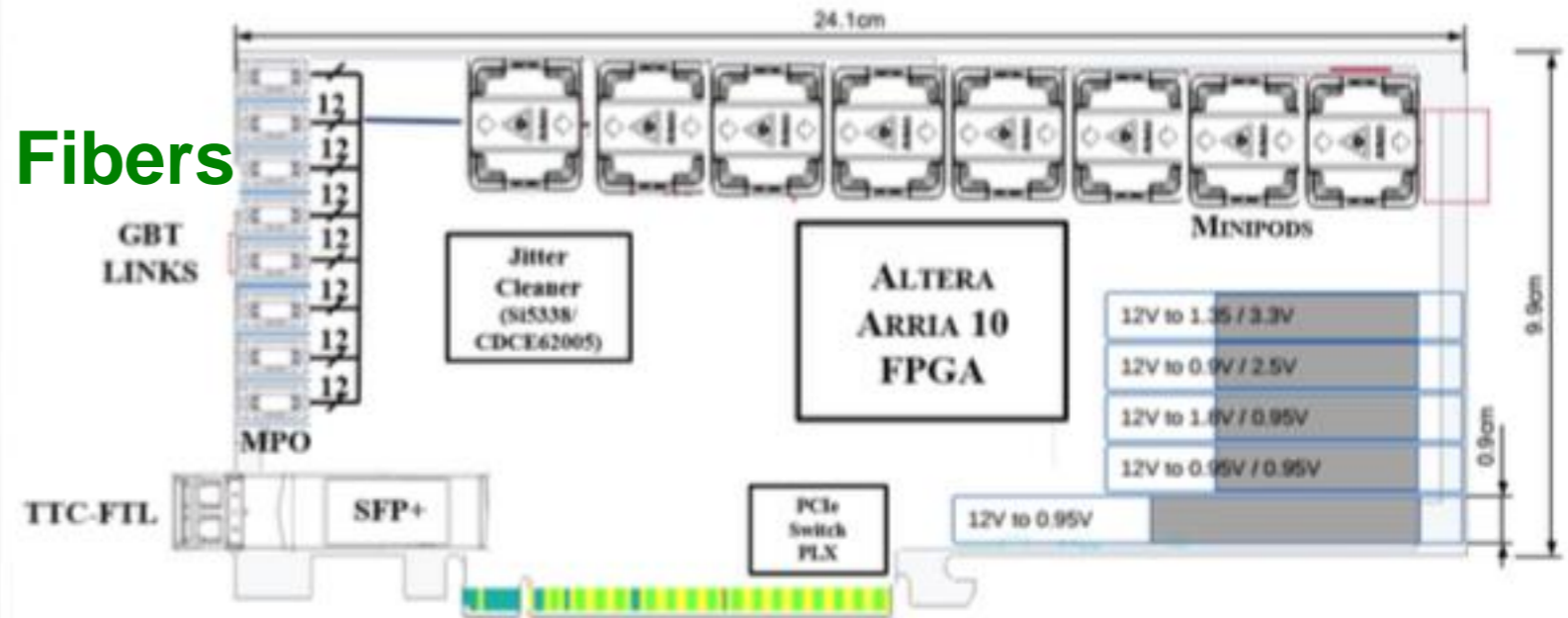Long run from Hall to Rack Room over custom CERN optical link

ALICE Common Readout Units

PCI express card

Avago optical engines

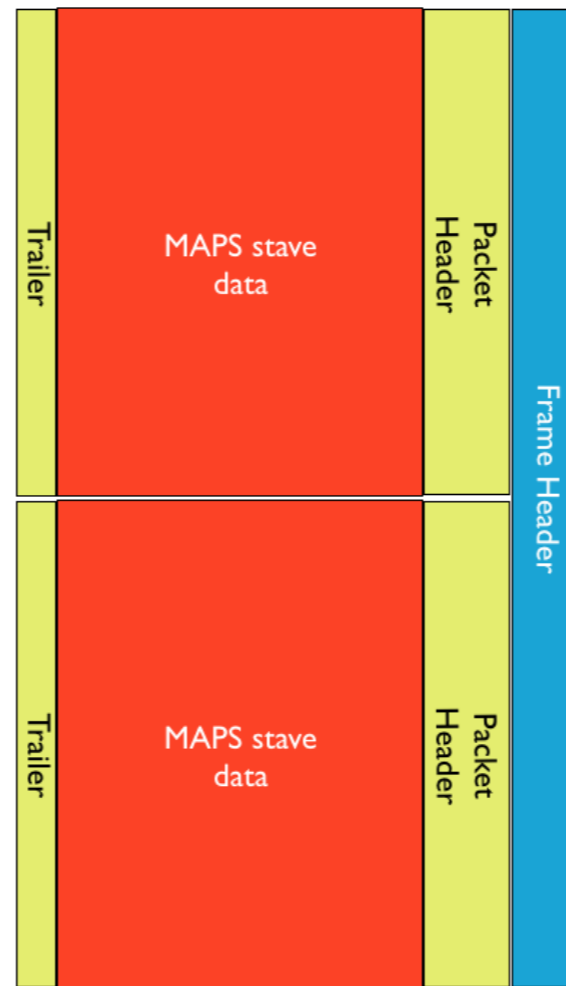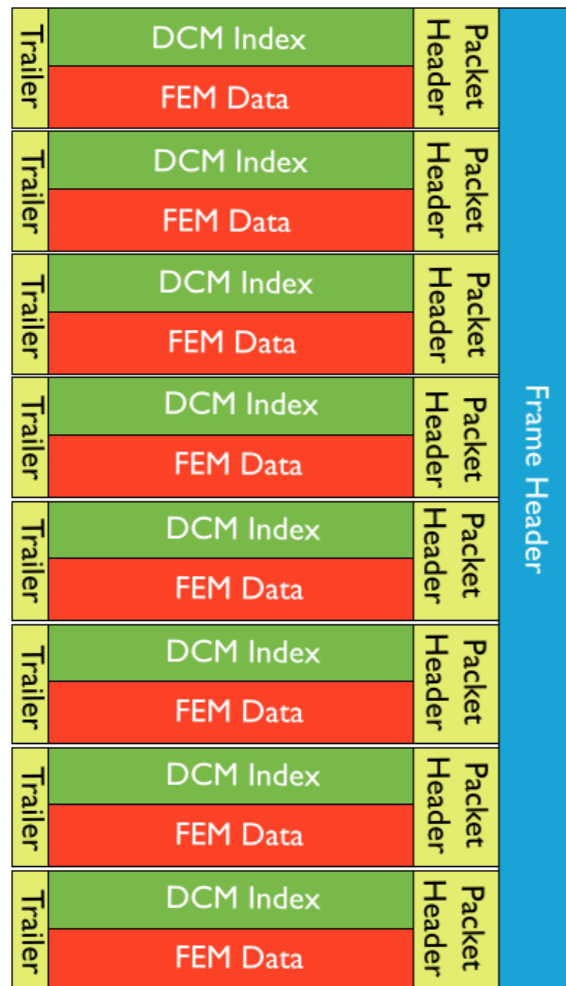(a) PCie40.   (b) PCIe40 Schematic.

Figure 6. Selected candidate board for CRU development.

Each CRU reads out two Readout units,
also sends slow controls, trigger
CRU cards reside in CPU chassis

Data Stream Reformatting

Traditional sPHENIX Frame
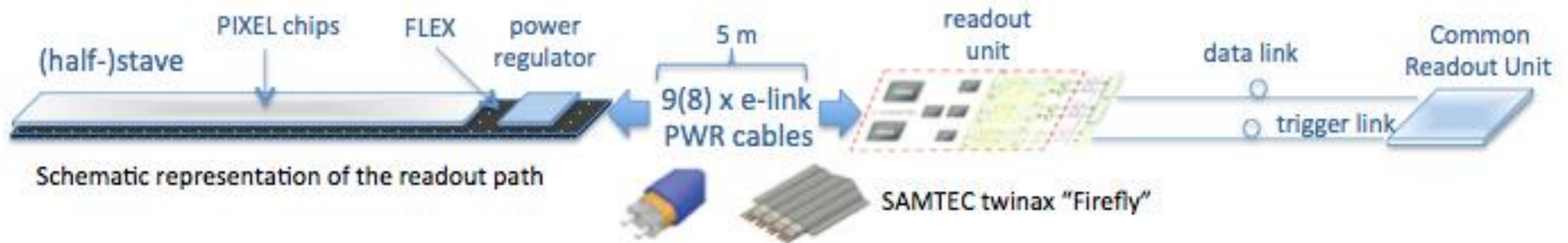
sPHENIX MAPS Common Readout Frame

Reformat options FPGA or CPU…

(a) PCie40.

ALICE Format Data

Transport Headers and Trailers

Au+Au Relative Bandwidth

ALICE ITS IB is physical signal dominated

Event multiplicity reduction: RHIC / LHC = 7000/20000 = 0.35
Collision rate increase: RHIC / LHC = 200 kHz / 150 kHz = 1.33

Continuous Stave-to-ROU link is ~50% bandwidth of ALICE ITS IB

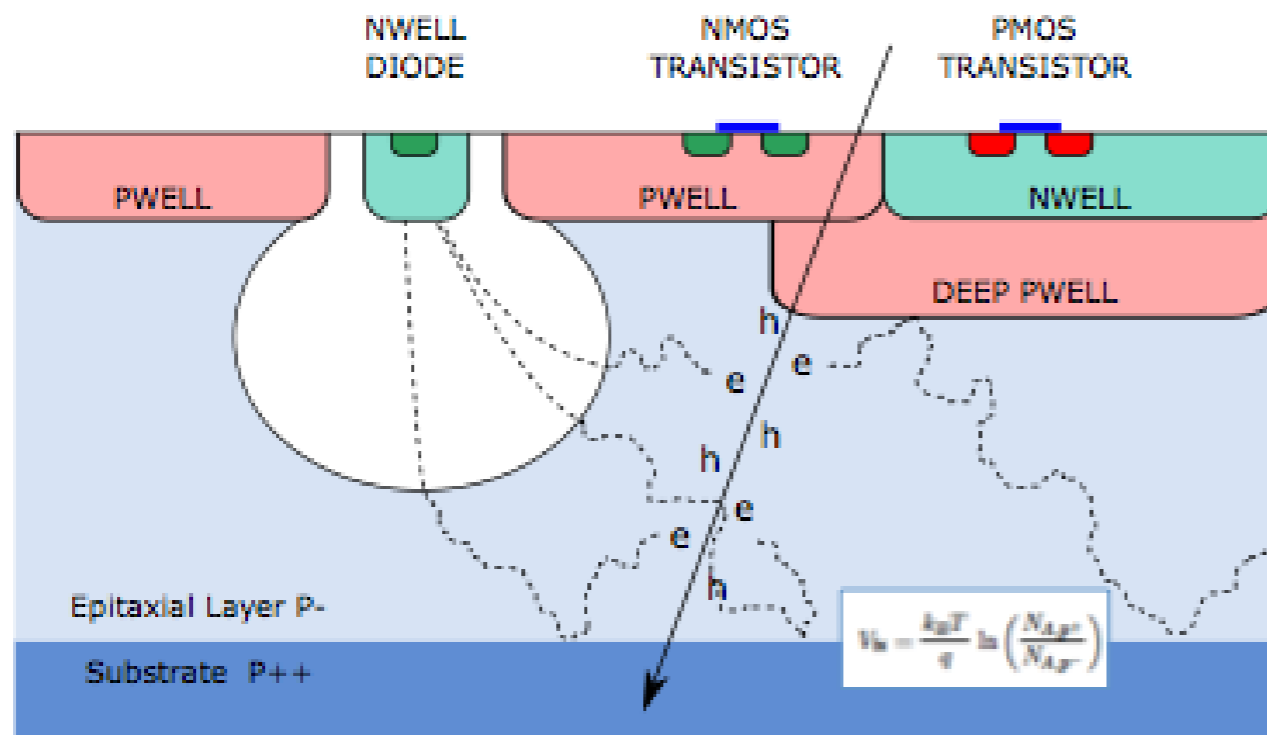**Trigger rate reduction:** RHIC / LHC = 15 kHz / 50 kHz = 0.30

Triggered ROU-to-CRU link is only ~15% bandwidth of ALICE ITS IB

Backups

ALPIDE Pixel Technology

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process
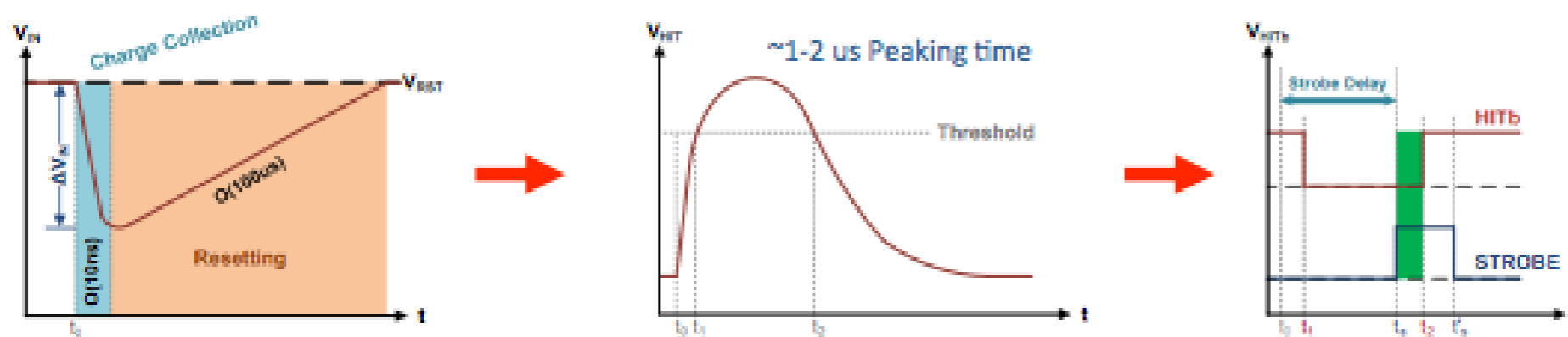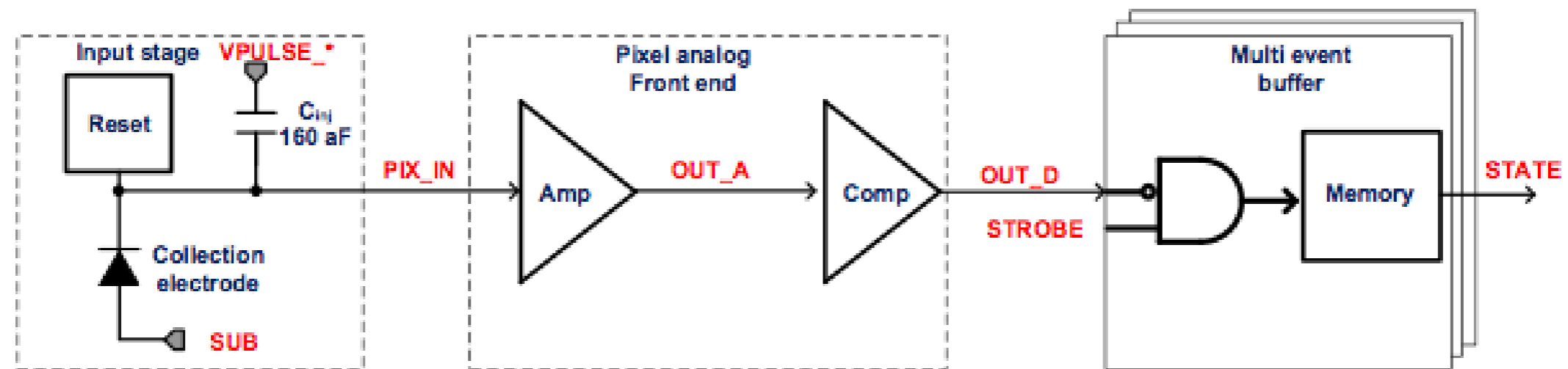

Tower Jazz 0.18 μm CMOS

- feature size   180 nm
- metal layers   6
- gate oxide   3nm

substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

▶ High-resistivity (> 1kΩ cm) p-type epitaxial layer (18μm to 30μm) on p-type substrate

▶ Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance

▶ Application of (moderate) reverse bias voltage to substrate (contact from the top) can be used to increase depletion zone around NWELL collection diode

▶ Deep PWELL shields NWELL of PMOS transistors to allow for full CMOS circuitry within active area

ALPIDE Operation

Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with ~1-2µs peaking time
- Threshold is applied to form binary pulse
- Hit is latched into a (3-bit) memory if strobe is applied during binary pulse

ultra low-power front-end circuit
40nW / pixel

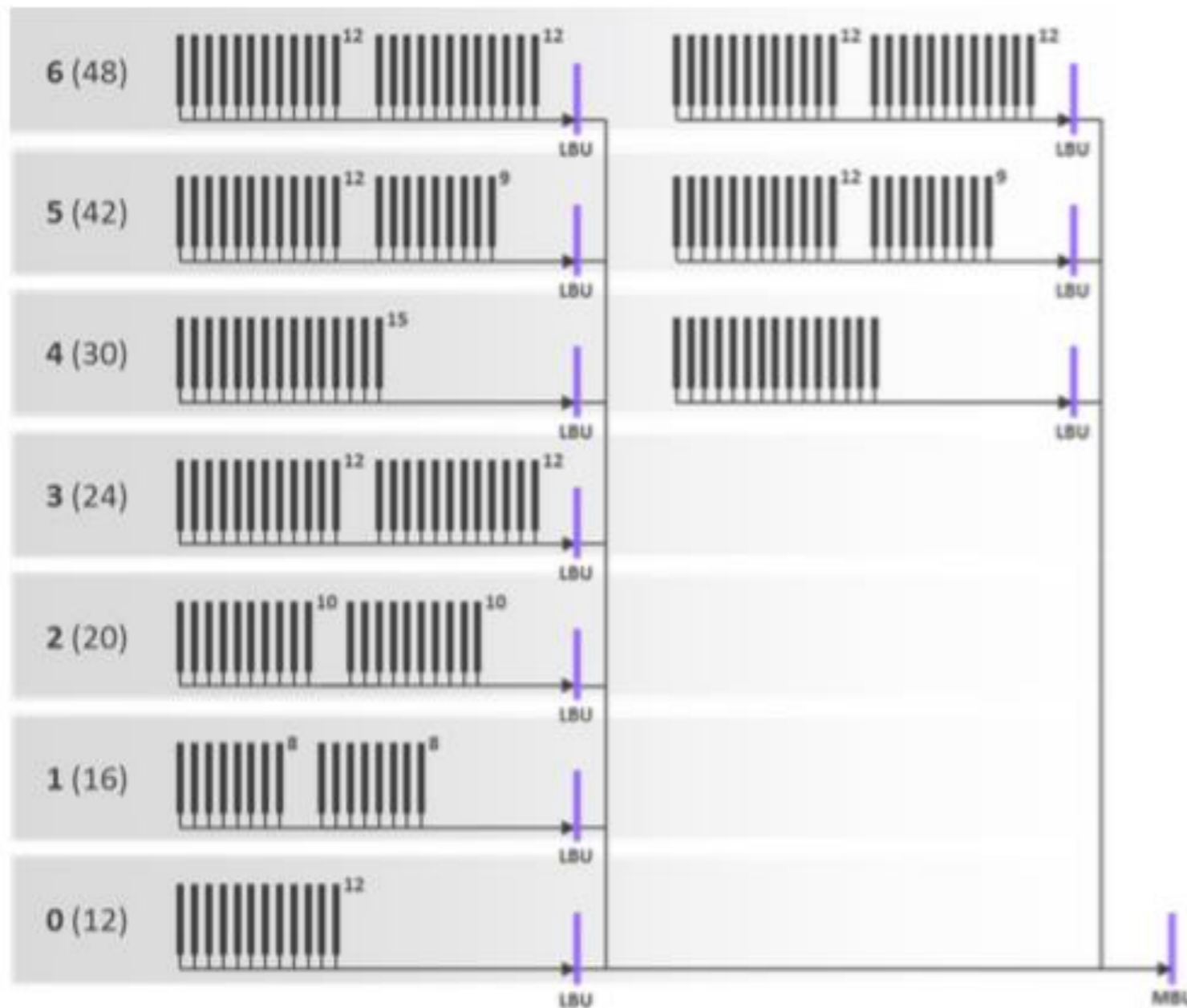# ALPIDE Readout

ALPIDE

continuous
or
external trigger
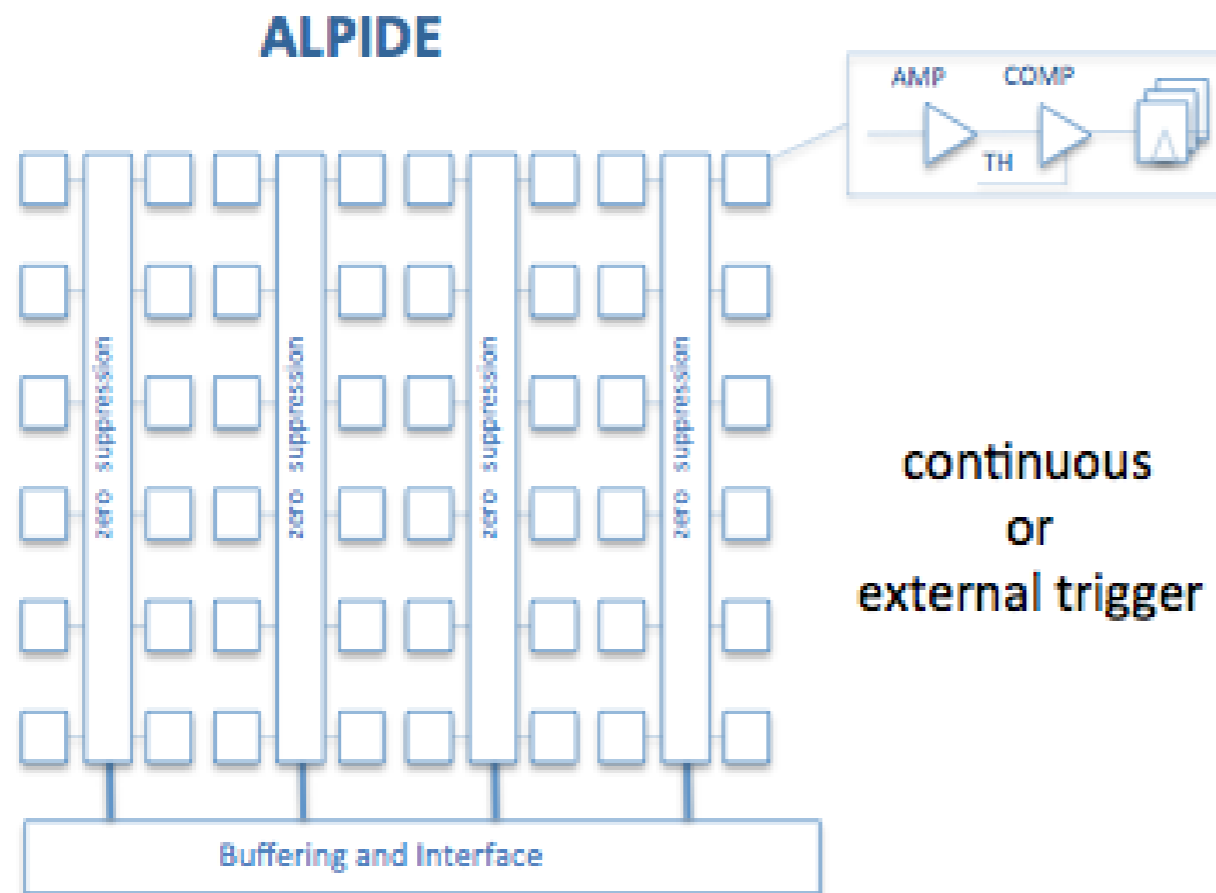
Architecture

▶ In-pixel amplification

▶ In-pixel discrimination

▶ In-pixel (multi-) hit buffer

▶ In-matrix sparsification

Key Features

⊙ 28 μm x 28 mm pixel pitch

⊙ Continuously active, ultra-low power front-end (40nW/pixel)

⊙ No clock propagation to the matrix ➔ ultra-low power matrix readout (2mW whole chip)

⊙ Global shutter (<10μs): triggered acquisition or continuous

Optional Busy Back

Figure 56 – Busy signal routing with local and master busy units highlighted in purple.

Busy sensors record state in data stream for offline use

ALICE considering busy reporting

Local Busy Units (LRU) in RO crate can be programmed to report back busy signals

Likely unnecessary for sPHENIX